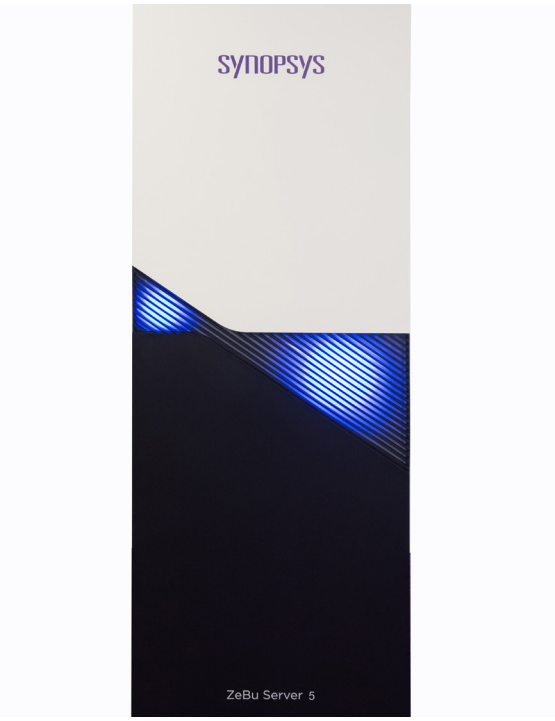
SYNOPSYS®

SPEC SHEET

ZeBu Server 5

Industry's Most Scalable HW-Assisted Verification System



ZeBu Server 5 System: 3.8B gates

ZeBu Server 5

- 2X higher performance over previous generation ZeBu Server
- Industry's largest capacity, scalable from 60 million gates to designs over 30 billion gates
- Industry's lowest total cost of ownership—up to 10X lower power consumption with half the datacenter footprint
- Unmatched hardware reliability versus competitive platforms
- Enables bring-up of complex software workloads required for automotive, 5G, networking, artificial intelligence and datacenter SoCs
- Delivers software innovations for faster compile, advanced debug, power analysis, simulation acceleration and hybrid with virtual prototypes

Synopsys ZeBu® Server 5 builds on the proven ZeBu architecture with 2X the performance over competing solutions, to enable system-on-chip (SoC) verification and software bring-up, and to address the exploding verification requirements of automotive, 5G, networking, artificial intelligence (AI), and datacenter SoCs. ZeBu Server 5 offers up to 10X lower power consumption with half the datacenter footprint, delivering the industry's lowest cost of ownership. In addition, Synopsys ZeBu Server 5 delivers software innovation for faster compile, advanced debug, power analysis, simulation acceleration, and hybrid.

For more information about ZeBu systems contact your Synopsys representative or visit www.synopsys.com/zebu

ZeBu Hardware	Synopsys ZeBu Server 5
Max Capacity	Up to 3.8 billion gates, single rack
	Up to 15 billion gates, 5 connected racks
	Up to 30 billion gates, 10 connected racks
Max Power	< 6 kW / billion gates
Dimensions	H: 214cm, W: 82cm, D: 129cm
Weight	< 650Kg
ZeBu Software	
Language Support	Verilog, VHDL, SystemVerilog, EDIF gate-level, SystemVerilog assertions, OVL, SystemC
Use Modes	Hybrid with virtual prototypes, simulation acceleration, power analysis, synthesizable test bench, transaction-based emulation, in-circuit emulation, virtual host and device models, virtual tester
Low Power Verification	IEEE 1801 UPF, power domains, power gating, isolation, retention
Power Analysis	RTL average power, gate level average and cycle power
Debug	View all signals anytime with unlimited waveform upload onto host, or limited waveform depth capture by using interactive/batch waveform reconstruction within Verdi
Vertical Solutions	More than 125 protocol, use case, and vertical market solutions spanning transactors, memory models, hybrid solutions, virtual system adaptors and speed adaptors